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09/164,123	09/30/1998	ALBRECHT MAYER	GR-97-P-2681	6288

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EXAMINER
MALDONADO, JULIO J

ART UNIT	PAPER NUMBER
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/164,123	Applicant(s) MAYER, ALBRECHT	
	Examiner Julio J. Maldonado	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 16-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 7 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simmons et al. (U.S. 4,714,949) in view of Hatanaka (U.S. 5,587,598) and Emori (0115143 A2).

In reference to claims 1 and 18, Simmons et al. (Fig.1-4) in a related art to form electrostatic discharge (ESD) protections teach providing a lower circuitry having a terminal (11) and a signal terminal (13); forming an electrically conductive connection (9) between the terminal (11) and the signal terminal (13) of the lower integrated circuit; providing a protective structure (3) that becomes conductive to dissipate electrostatic discharges; providing an upper circuitry having a terminal (23); electrically connecting the signal terminal (13) of the lower circuitry to the terminal (23) of the upper circuitry; and severing the electrically conductive connection (9) between the terminal (11) and the signal terminal (13) of the lower circuitry using an energy pulse (column 2, line 48 – column 3, line 36).

Simmons et al. fail to teach forming a first and second integrated circuit having a terminal coupled to the protective structure and disposing the first and second integrated circuit adjacent to one another. However, Hatanaka (Fig.1-5) in a related art to ESD devices shows a semiconductor device with charge up prevention function

including a first and second integrated circuit (20) having a terminal coupled to the protective structure (23, 24) and disposing the first and second integrated circuit adjacent to one another (column 3, line 5 – column 4, line 67). Therefore, it would have been obvious to one of ordinary skill in the art to include the first and second integrated circuit adjacent to one another, and coupling at least one terminal of the second integrated circuit with the protection device as taught by Hatanaka into the ESD device of Simmons et al., since the protective structure controls potential variations of the device (column 4, line 61 – column 5, line 4).

4 Simmons et al. in combination with Hatanaka fail to teach connecting the terminal of the first integrated circuit to a terminal of the package and subsequent to connecting the terminal of the first integrated circuit to the terminal of the package, severing the electrically conductive connection. However, Emori (Fig.1-3) in a related art to electrostatic breakdown prevention circuits teaches forming protective structures (D1, D2); coupling the protective structures (D1, D2) to the first integrated circuit (101, 102); connecting the terminal of the first integrated circuit (101, 102) to a terminal of the package (P) and subsequent to connecting the terminal of the first integrated circuit (101, 102) to the terminal of the package (P), severing the electrically conductive

16 connection (page 3, lines 3-8 and page 4, lines 2-8). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include the connecting the integrated circuit prior to sever the electrically conducting connection as taught by Emori into the combination of Simmons et al. and Hatanaka, since this

reduces the operation speed decrease caused by the protective structure (page 3, line 35 – page 4, line 12).

In reference to claim 2, Simmons et al. in combination with Hatanaka and Emori teach severing the electrically conductive connection by applying an electrical current pulse to the terminal of the second integrated circuit (Simmons et al. column 3, lines 30-36, Hatanaka, column 4, lines 18-24 and Emori, page 4, lines 2-8).

In reference to claim 3, Simmons et al. teach forming electrically conductive connection (9) with a portion of reduced cross sectional area as compared to the rest of the connection (Fig.2b); and dimensioning the portion to dissipate electrostatic discharges between the terminal (11) of the integrated circuit and to be severed during the application of the energy pulse in the severing step (column 2, line 48 – column 3, line 36).

In reference to claims 4, 7, 16 and 17, Simmons et al. in combination with Hatanaka and Emori teach applying an electrical current pulse (Simmons et al., column 3, lines 30-36) or a laser beam (Hatanaka, column 4, lines 25-29) to the terminal of the second integrated circuit; and that the disposing step is performed so that the terminal of the second integrated circuit is not covered by the first integrated circuit.

3. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simmons et al. ('949) in view of Hatanaka ('598) and Emori ('143 A2) as applied to claims 1-4, 7 and 16-18 above, and further in view of Kuriyama (U.S. 5,682,057).

In reference to claims 5 and 6, Simmons et al. in combination with Hatanaka and Emori teach that the first integrated circuit is not accessible from outside of the package

(Simmons et al., Fig.3). Simmons et al. in combination with Hatanaka and Emori fail to teach disposing the first and second integrated circuits in a package having terminal pins so that the signal terminal of the first integrated circuit is not accessible from outside of the package; connecting the terminal of the first integrated circuit and the terminal of the second integrated circuit to a respective terminal pin of the package; and that the severing step is performed after the step of connecting the respective terminals to the respective terminal pins. However, Kuriyama (Fig.1-2) in a related art to ESD devices teaches disposing the first and second integrated circuits (3, 7) in a package (17) having terminal pins (4, 5) so that the signal terminal (3b) of the first integrated circuit (3) is not accessible from outside of the package (17); connecting the terminal (3c) of the first integrated circuit (3) and the terminal (11) of the second integrated circuit (7) to a respective terminal pin (5) of the package (17); and that the severing step (column 3, lines 55-67) is performed after the step of connecting the respective terminals (3b, and 12) and to the respective terminal pins (4 and 5) (column 3, lines 4-49). Therefore, it would have been obvious to one of ordinary skill in the art to include packaging steps as taught by Kuriyama into the combination of Simmons et al., Hatanaka and Emori, since this protects the fuse element from being prematurely melt-cut by passage of a normal operating current and makes the device less likely to encounter unexpected mechanical damages (column 4, lines 1-10).

4. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simmons et al. ('949) in view of Hatanaka (''598), Kuriyama ('057) and Bozso (U.S. 5,760,478).

In reference to claim 8, Simmons et al. (Fig.1-4) in a related art to form electrostatic discharge (ESD) protections teach providing a lower circuitry having a surface; disposing first and second terminal pads (11, 13) on the surface of the lower circuitry; forming an electrically conductive connection (9) between the first (11) and second (13) terminal pads of the lower circuitry; providing an upper circuitry having a surface; providing a protective structure (3) that becomes conductive to dissipate electrostatic discharges; and severing the electrically conductive connection (9) using an energy pulse (column 2, line 48 – column 3, line 36).

Simmons et al. fail to teach forming a first and second integrated circuit, said integrated circuits having a surface; disposing the first and second terminal pads on the surface of the second integrated circuit; and electrically coupling at least the first terminal pad of the second integrated circuit to the protective structure. However, Hatanaka in a related art to form ESD devices teaches forming a first and second integrated circuit, said integrated circuits having a surface; disposing the first and second terminal pads on the surface of the second integrated circuit; and electrically coupling at least the first terminal pad of the second integrated circuit to the protective structure (column 3, line 5 – column 4, line 67). Therefore, it would have been obvious to one of ordinary skill in the art to include the first and second integrated circuit adjacent to one another, and coupling at least one terminal of the second integrated circuit with the protection device as taught by Hatanaka into the ESD device of Simmons et al., since the protective structure controls potential variations of the device (column 4, line 61 – column 5, line 4).

Simmons et al. in combination with Hatanaka fail to teach disposing the surfaces of the first and second integrated circuits longitudinally adjacent one another; and electrically joining at least one of the first and second terminal pads of the first integrated circuit to one of the first and second terminal pads of the second integrated circuit. However, Kuriyama (Fig.1-2) in a related art to ESD devices teaches disposing the surfaces of the first (3) and second (7) integrated circuits longitudinally adjacent one another; and electrically joining at least one of the first (3b) and second (3c) terminal pads of the first integrated circuit (3) to one of the first (11) and second (12) terminal pads of the second integrated circuit (7) (column 3, lines 55-67). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to dispose of the integrated circuits as taught by Kuriyama into the combination of Simmons et al. and Hatanaka, since this protects the devices in the load circuit (column 3, lines 55-67).

Simmons et al. in combination with Hatanaka and Kuriyama fail to teach disposing the surfaces of the first and second integrated circuits longitudinally adjacent one another so that the first and second terminal pads of the second integrated circuit are not covered by the first integrated circuit. However, Bozso et al. (Fig.6) in a related art to flip-chips teach disposing the surfaces of the first and second integrated circuits longitudinally adjacent one another so that the first and second terminal pads of the second integrated circuit are not covered by the first integrated circuit (column 5, lines 30-51). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to dispose the surfaces of the integrated circuits as taught by

Boszo in the combination of Simmons et al., Hatanaka and Kuriyama, since this provides means for external connection, resulting in a less expensive package (column 5, lines 36-39 and 52-57).

In reference to claims 9-11, Simmons et al. in combination with Hatanaka, Kuriyama and Bozso et al. teach that the electrically joining step is performed using an electrically conductive solderable or adhesive material; and including electrically joining the other one of the first and second terminal pads of the second integrated circuit (Hatanaka, column 3, line 5 – column 6, line 11).

Response to Arguments

5. Applicant's arguments with respect to claims 1-11 and 16-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432** . The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone

are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

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